*SSCS Distinguished Lecture - 1*

# The Innovation is in the Mind – The Converging Trajectories of IT, Neuro and Nano

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## Abstract

The brain is an amazingly complex and efficient machine. While it may not be considered "general purpose" in terms of its computational capabilities, it performs a set of functions such as feature extraction, classification, synthesis, recognition, learning, and higher-order decision-making amazingly well.

Yet the dynamic behavior of the brain at large is still marginally understood. One of the major charters in the neuroscience community for the next decade is to create a dynamic map of the brain (as articulated by the Obama administration). Doing so will require the most advanced imaging capabilities operating at the scale of 10's of microns. Recent advances in microscopic sensing, processing and communications are leading to brain-machine interfaces that may be able to observe thousands if not millions of active neurons in vivo. These nano-morphic systems represent the frontier in miniaturization and integration of electronic information processing systems.

This whole effort may in turn have some interesting repercussions on how information-processing systems themselves are conceived in the nanoscale regime. Neuro-inspired processing presents an attractive alternative to the classical Von-Neumann computing paradigm in deeply scaled regimes: it thrives on randomness and variability, processing is performed in the continuous or discrete domains, and massive parallelism, major redundancy and adaptivity are of essence. Computational paradigms inspired by neural information processing hence may lead to energy-efficient, low-cost, dense and/or reliable implementations of the functions the brain excels at.

In this presentation, we will explore both sides of this neuroscience-information technology interaction. One thing is for sure – the joint future will be exciting.

## Speaker's Biography

Jan Rabaey received his Ph.D degree in applied sciences from the Katholieke Universiteit Leuven, Belgium. In 1987, he joined the faculty of the Electrical Engineering and Computer Science department of the University of California, Berkeley, where he now holds the Donald O. Pederson Distinguished Professorship.

He is currently the scientific co-director of the Berkeley Wireless Research Center (BWRC), as well as the founding director of the Berkeley Ubiquitous SwarmLab.

He is the recipient of a wide range of major awards, , amongst which the IEEE CAS Society Mac Van Valkenburg Award, the European Design Automation Association (EDAA) Lifetime Achievement award, and the Semiconductor Industry Association (SIA) University Researcher Award. He is an IEEE Fellow and a member of the Royal Flemish Academy of Sciences and Arts of Belgium. In 2012, he received an honorary doctorate from the University of Lund, Sweden. He has been involved in a broad variety of start-up ventures.

His research interests include the conception and implementation of next-generation integrated wireless systems over a very broad range of applications, as well as exploring the interaction between the cyber and the biological world.

## *SSCS Distinguished Lecture – 2*

# K-Delta-1-Sigma Analog-to-Digital Converters

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## Abstract

As CMOS technology shrinks the transistor speed increases enabling higher-speed communications and more complex systems. These benefits come at the cost of decreasing inherent device gain, increased transistor leakage currents, and additional mismatches due to process variations. All of these drawbacks influence the design of quality analog-to-digital converters (ADCs) in nanometer scale CMOS processes. To move towards a manufacturable ADC topology in nanometer CMOS the K-Delta-1-Sigma (KD1S) modulator-based ADC was developed. The architecture has the potential to provide a solution to high-speed data conversion in nano-CMOS including applications which traditionally employ the Pipeline and Flash ADC architectures. This talk provides an overview of the KD1S ADC and provides experimental results verifying the data converter's operation.

## Speaker's Biography

Russel Jacob (Jake) Baker (S'83-M'88-SM'97-F'13) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas, in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno in 1993. His Google scholar profile is located here.

From 1981 to 1987 he served in the United States Marine Corps Reserves. From 1985 to 1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada test site. During this time he designed over 30 electronic and electro-optic instruments including high-speed fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs, data converters, streak-camera sweep circuits, Pockell's cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1993 to 2000 he served on the faculty in the department of electrical engineering at the University of Idaho. In 2000 he joined a new electrical and computer engineering program at Boise State University where he served as department chair from 2004 to 2007. At Boise State he helped establish graduate programs in electrical and computer engineering including, in 2006, the university's second PhD degree. In 2012 he joined the faculty

at the University of Nevada, Las Vegas where his research focuses on the design of diagnostic instrumentation for scientific research, integrated electrical/biological circuits and systems, methods to fabricate trusted integrated circuits, array (memory and displays) circuit design, low-power interconnect techniques, communication circuit design, and the delivery of online engineering education.

Since 1993 he has consulted for various companies and laboratories including: Aerius Photonics, Amkor, Agere, AmTRAN, Arete' Associates, ASUS, Atmel, Cirque, Contour Semiconductor, Creative Industries, CSR, Dell, Elm Technology, Elpida, Envision Peripherals, FLIR, Fujitsu, Funai Electric, GSI Technology, Infineon, InvenSense, ITRAN Communications, Kingston Technology, the Lawrence Berkeley Laboratory, Lockheed-Martin, LSI, Marvell, Micron, MediaTek, Nascentric, OmniVision, Oracle, Rendition, Samsung, Sanyo, SK Hynix, Sun, Target, Top Victory Electronics, Tower Semiconductor, TPV, Vizio, Xilinx, and Zoran.

Professor Baker holds over 200 granted or pending patents in integrated circuit design. Among his inventions is the K-Delta-1-Sigma modulator topology used in the Baker analog-to-digital converter. He is a member of the engineering honor society Eta Kappa Nu, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society, the 2007 Frederick Emmons Terman Award, and the 2011 IEEE Circuits and Systems (CAS) Education Award.

He also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau (2007-present), as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University (2012-present), as the Technology Editor for the IEEE Solid-State Circuits Magazine (2012-present), and as a Distinguished Lecturer for the SSCS (2013-2014).

## *SSCS Distinguished Lecture – 3*

# Silicon-based Circuits and Systems at the Terahertz Frontier

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## Abstract

The push for novel applications in the sub-mmWave region of the electromagnetic spectrum has raised the bar on RF circuit design and characterization. Continued device scaling enables circuits to operate at frequencies so high that contact-less wafer testing (in free space) is the last resort. This talk will summarize this frontier. It follows practical CMOS and SiGe BiCMOS design examples including 0.5 THz high-power oscillators, sub- harmonically operated receivers and transmitters up to 0.8 THz, and broadband direct detectors for active imagers running well beyond 1 THz.

## Speaker's Biography

Ullrich R. Pfeiffer received the diploma degree in physics and the Ph.D. in physics from the University of Heidelberg, Germany, in 1996 and 1999 respectively. In 1997 he worked as a research fellow at the Rutherford Appleton Laboratory, Oxfordshire England.

From 1999-2001 he was working as a Postdoctoral Researcher, at the University of Heidelberg on real-time electronics for particle physics experiments at the European Organization for Nuclear Research (CERN), Switzerland.

From 2001 to 2006 he was with the IBM T.J. Watson Research Center where his research involved RF circuit design, power amplifier design at 60GHz and 77GHz, high-frequency modeling and packaging for millimeter-wave communication systems.

In 2007 he received a European Young Investigator Award and lead the THz electronics group at the Institute of High-Frequency and Quantum Electronics at the University of Siegen, Germany.

Since 2008 he holds the High-frequency and Communication Technology chair at the University of Wuppertal, Germany.

He was the co-recipient of the 2004 and 2006 Lewis Winner Award for Outstanding Paper at the IEEE International Solid-State Circuit Conference, the co-recipient of

the 2006 IBM Pat Goldberg Memorial Best Paper Award, the 2008 EuMIC Best Paper Award, the 2009 Best RFIC Oral Paper Presentation, and the 2010 EuMC Microwave Prize, and the 2012 Jan Van Vessem Award for Outstanding European Paper at the 2012 IEEE International Solid-State Circuit Conference.

He is a Senior Member of IEEE, and serves on the technical program committee of the International Solid-State Circuits Conference, the European Solid-State Circuits Conference, the Bipolar/BiCMOS Circuits and Technology Meeting, the Silicon Monolithic Integrated Circuits in RF Systems Conference, and the European Microwave Integrated Circuits Conference.

He has authored and co-authored 100+ publications and has been principal inventor and co-inventor of 10+ US and international issued patents, relating to RF, millimeter-wave, terahertz communication/imaging circuits and sensors.